Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 5, 8-11, 13, 23-25, 27, 29, 35-38, 40-42 and 47 have been amended. Claims 2, 4, 6, 26, 39, 43 and 46 have been cancelled. Therefore, claims 1, 3, 5, 7-25, 27-38, 42, 44, 45 and 47 are presented for examination.

Claims 3, 7-9, 13, 29, 44, and 45 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants submit that the claims have been amended to appear in proper condition for allowance.

Claim 1 stands provisionally rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claim 1 of co-pending Application No. 10,676,478). Applicants submit that the non-statutory obviousness-type double patenting rejection has been obviated by the amendment to claim 1.

Applicants acknowledge that claims 12, 22, 28, 34 and 39 would be allowable if rewritten to include the features of the base claim and any intervening claims.

Claims 1-7, 9-11, 14, 17-18, 21, 23-27, 32-33, 35-37 and 41-47 stand rejected under 35 U.S.C. §102(e) as being anticipated by Naffziger et al. (U.S. Pub. No. 2003/0135694). Further, claims 15-16 and 30-31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger. Applicants submit that the present claims are patentable over Naffziger.

Naffziger discloses a compression engine for a cache memory subsystem that has a pointer into cache tag memory and cache data memory and an interface coupled to the pointer and capable of being coupled to cache tag memory, and cache data memory. The

interface reads tag information and uncompressed data from the cache and writes modified tag information and compressed data to the cache. The compression engine also has compression logic for generating compressed data and generating compression successful information, and tag line update circuitry for generating modified tag information according to the compression successful information and the tag information. See Naffziger at Abstract.

Claim 1 of the present application recites a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. Applicants submit that Naffziger does not disclose or suggest such a process. Therefore, claim 1 is patentable over Naffziger. Claims 3, 5 and 7-22 depend from claim 1 and include additional features. Thus, claim 3, 5 and 7-22 are also patentable over Naffziger.

Claims 23, 35 and 42 recite similar identical features described above with respect to claim 1. Accordingly, claims 23, 35 and 42 and their respective dependent claims are also patentable over Naffziger.

Claims 8 and 40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger and Yanai et al. (U.S. Patent No. 5,206,939). Applicants submit that the present claims are patentable over Naffziger even in view of Yanai.

Yanai discloses an apparatus and method for disk mapping and data retrieval includes a data storage medium on which has been stored a plurality of data records. See Yanai at Abstract. Nonetheless, Yanai does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an

offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger does not disclose or suggest such a feature. Thus, any combination of Naffziger and Yanai would also not disclose or suggest the feature. As a result, the present claims are patentable over Naffziger in view of Yanai.

Claims 13 and 38 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger and Gross (U.S. Pub. No. 2004/0255209). Applicants submit that the present claims are patentable over Naffziger even in view of Gross.

Gross discloses an embedded memory on an integrated circuit has a memory cell array equipped with replacement cells and mapping logic for electronically substituting the replacement cells for defective cells at least one location in the memory cell array. The memory also has programmable links for storing redundancy information in a compressed format, and decoding logic for decompressing the redundancy information and controlling the mapping logic. See Gross at Abstract.

However, Gross does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger does not disclose or suggest such a feature. Therefore, any combination of Naffziger and Gross would also not disclose or suggest the feature. Accordingly, the present claims are patentable over Naffziger in view of Gross.

Claim 19 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger and Wang et al. (U.S. Patent No. 6,507,895). Applicants submit that the present claims are patentable over Naffziger even in view of Wang.

Wang discloses an apparatus for memory access demarcation. Nevertheless, Wang does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger does not disclose or suggest such a feature. Thus, any combination of Naffziger and Wang would also not disclose or suggest the feature. Consequently, the present claims are patentable over Naffziger in view of Wang.

Claim 20 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Naffziger in view of Shimoi et al. (U.S. Patent No. 5,652,857). Applicants submit that the present claims are patentable over Naffziger even in view of Shimoi.

Shimoi discloses logic blocks which were swept out from a non-compression cache memory that are compressed by a compressing circuit and combined to a compression group (logic sector size) of a fixed length in which a plurality of compression data are collected by a compression group forming unit. See Shimoi at Abstract. However, Shimoi does not disclose or suggest a process wherein if a compression bit indicates a cache line is compressed a companion bit is treated as a part of an offset and if the compression bit indicates the cache line is not compressed the companion bit is considered a component of address tag bits. As discussed above, Naffziger does not disclose or suggest such a feature. Thus, any combination of Naffziger and Shimoi would also not disclose or suggest the feature. Therefore, the present claims are patentable over Naffziger in view of Shimoi.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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